WHAT IS CLAIMED IS:

1. An electronic device testing system comprising:

a tester operable to generate test data and apply the test data to the electronic device to determine the response of the electronic device;

a capture interface operable to capture the test data communicated to the electronic device by the tester;

a compression engine in communication with the capture interface and operable to compress the test data; and

memory in communication with the compression engine and operable to save the compressed test data.

2. The system of Claim 1 further comprising:

a de-compression engine interfaced with the memory and operable to de-compress the test data; and

an analyzer interfaced with the de-compression engine and operable to analyze the de-compressed test data to determine the test data source of an electronic device error response.

3. The system of Claim 2 wherein the test data comprises plural cycles including empty cycles not associated with the electronic device error response, and wherein the analyzer is further operable to generate a test program that reduces the empty cycles of the test data.

4. The system of Claim 1 wherein the tester is further operable to run the test program on production electronic devices to detect the error response.

5. The system of Claim 1 wherein the tester comprises a vector generator operable to generate vector test data.

6. The system of Claim 5 wherein the electronic device comprises a memory device operable to store data fields according to address and control

information and the vector generator generates memory vectors for storage on the memory device.

7. The system of Claim 6 wherein the compression engine further comprises:

a compressor having plural comparison modules, each comparison module having a width adapted for comparing data field, address or control information and a depth for comparing predetermined cycles of test vectors, the comparison modules operable to represent test vectors having matching data field, address or control information with a representation having a reduced size to output compressed vectors having variable lengths;

a reformater interfaced with the comparison modules and operable to reformat the compressed vectors of the comparison modules as concatenated words of similar length.

8. The system of Claim 7 wherein the compressor further comprises repeating vector detection logic operable to detect repeating test data patterns and to represent the repeating test data patterns as a word having the repeating value and a counter for the number of times the value repeats.

9. The system of Claim 1 wherein the memory further comprises:

plural memory motherboards;

a memory parser associated with each memory motherboard;

plural memory controllers associated with each memory parser; and

plural memory storage devices associated with each memory controller;

wherein the memory parser coordinates with its associated memory controllers to store test data on plural memory storage devices in sequence so that the memory storage devices operate on a lower clock speed than the test data generation clock speed.

10. A method for testing electronic devices, the method comprising:

generating test data for application to the electronic device;

communicating the test data to the electronic device through an interface;
capturing the test data communicated to the electronic device;
compressing the captured test data;
storing the compressed test data;
detecting an error response by the electronic device to the test data; and
analyzing the compressed test data to identify the source of the error response.

11. The method of Claim 10 wherein the electronic device comprises a memory device and generating test data further comprises generating vectors of memory test data for storage on the memory device, the memory test data having data field, address and control information.

12. The method of Claim 11 wherein detecting an error further comprises:
reading test data stored on the memory device;
comparing the read test data with the test data written to the memory device; and
detecting an error if the read test data differs from the written test data.

13. The method of Claim 11 wherein compressing the test data further comprises:
comparing the data field, address and control information of a vector with the data field, address and control information of a predetermined number of previous vectors to identify matches in one or more of the data field, address and control information; and
representing matches with defined opcodes that reduce the size of the vector.

14. The method of Claim 11 wherein compressing the test data further comprises:
detecting repeat patterns; and
representing the repeat patterns with the repeated value and a count of the number of repeats of the repeat value.

15. The method of Claim 10 wherein storing the compressed test data further comprises coordinating storage of the test data in plural storage devices so that the storage devices operate at a slower clock speed than the clock speed associated with the generation of the test data.

16. The method of Claim 10 wherein analyzing the test data further comprises:

de-compressing the compressed test data to replay the test data applied to the electronic device; and

passing the replayed test data through a logic analyzer to determine the applied test data that generated an error response.

17. The method of Claim 16 wherein analyzing the test data further comprises generating a test program to detect the error response by generating test data cycles associated with the error response and reducing test data cycles not associated with the error response.